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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,964	03/11/2004	Philip J. Tait	P18323	9017

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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 03/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,964	TAIT ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination.

2. The preliminary amendment filed on 09/29/2004 has been received and entered in the application.

Specification

3. The disclosure is objected to because of the following informalities:

It should be stated as "... example, device adapter 144 ... where a reply block comprise a transaction I.D.. A transaction I.D. circuitry 126 may ..." in lines 4-6 of paragraph [0027] of the specification instead of "... example, device adapter 144 ... where a reply block comprise a transaction I.D. circuitry 126 may ..." as disclosed in this application.

Appropriate correction is required.

4. This application does not contain a Brief Summary of Invention as set forth in 37 CFR 1.73.

The summary is separate and distinct from the abstract and is directed toward the invention rather than the disclosure as a whole.. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and

gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention. See MPEP § 608.01(d).

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 16-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 16-20 are not limited to only tangible embodiments. In view of applicants' disclosure (Specification, paragraphs [0017]-[0018]), a machine-readable medium is not limited to only tangible embodiments, instead being defined as including both tangible embodiments (e.g. floppy diskettes, optical disks, CD-ROMs (Compact Disc-Read Only Memories), magneto-optical disks, ROMs (Read Only Memories), RAMs (Random Access Memories), EPROMs (Erasable Programmable Read Only Memories), EEPROMs (Electrically Erasable Programmable Read Only Memories), magnetic or optical cards, flash memory) and intangible embodiments (e.g. carrier wave(s)). As such, these claims are not limited to statutory subject matter and are therefore non-statutory.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 6, 11 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Overney (USPN: 2003/0188180).

As per claim 1, Overney teaches a method for ensuring the data integrity during file(s) transfer. Overney teaches that the method comprising in response to a data read request for requested data, allocating an area of memory to the requested data, the memory area being divided into at least one memory chunk, i.e. receiving and storing a data file from a trusted source (e.g. see the abstract). Overney further teaches that the method comprising the step of writing a seed value to one or more of the at least one memory chunk (i.e. the verification station); and in response to completion of at least one write transaction corresponding to the data read request, for each of the one or more memory chunks having a seed value, validating the integrity of each of the at least one write transaction based, at least in part, on the seed value, i.e. verifying the integrity of the data file after the data file is written (e.g. see the abstract).

As per claims 6, 11 and 16, see arguments with respect to the rejection of claim 1. Claims 6, 11 and 16 are also rejected based on the same rationale as the rejection of claim 1.

7. Claims 1-4, 6-9 and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Horst et al. (USPN: 5,867,501) hereinafter, Horst.

As per claim 1, Horst teaches a method comprising: in response to a data read request for requested data: allocating an area of memory to the requested data, the memory area being divided into at least one memory chunk (i.e. the area of the memory) (e.g. see Col. 29, lines 53-56). Horst further teaches about writing a seed value (i.e. the CRC bits) to one or more of the at least one memory chunk (e.g. see Col. 5, lines 37-40); and in response to completion of at least one write transaction corresponding to the data read request, for each of the one or more memory chunks having a seed value, validating the integrity of each of the at least one write transaction based, at least in part, on the seed value (e.g. see Col. 5, lines 40-48).

As per claim 2, Horst teaches the claimed invention as described above and furthermore, Horst teaches that the validating the integrity of a given one of the at least one write transaction comprises, for a given memory chunk: determining if the memory chunk includes the seed value (i.e. the CRC bits); and if the memory chunk includes the seed value, determining that a transmission error occurred (i.e. by checking the CRC bits and declaring the transmission error if the CRC bits do not match) (e.g. see Col. 5, lines 44-47).

As per claim 3, Horst teaches the claimed invention as described above and furthermore, Horst teaches that the determining if the memory chunk includes the seed value comprises determining if the memory chunk (i.e. the area of the memory) includes the seed value (i.e. the CRC bits) at specified bits (i.e. the 4-bytes at the LSB side,

"CRC" field as shown in Fig. 3A) of the memory chunk (e.g. see Fig. 3A and Col. 17, lines 19-23).

As per claim 4, Horst teaches the claimed invention as described above and furthermore, Horst teaches that the method additionally comprising modifying the seed value (i.e. recalculating the CRC bits) if it is determined that a transmission error occurred (e.g. see Col. 22, line 65 – Col. 23, line 11).

As per claims 6-9, see arguments with respect to the rejection of claims 1-5, respectively. Claims 6-9 are also rejected based on the same rationale as the rejection of claims 1-5, respectively.

As per claims 16-19, see arguments with respect to the rejection of claims 1-5, respectively. Claims 16-19 are also rejected based on the same rationale as the rejection of claims 1-5, respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 5, 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horst in view of Klein (USPN: 2003/0191888).

As per claim 5, Horst teaches the claimed invention as described above. However, Horst does not teach that the size of the seed value is based on a specified

error rate of the device. Klein, on the other hand, teaches that the size of the seed value (i.e. the number of check bits) is based on a specified error rate of the device (i.e. the number of errors) (e.g. see paragraph [0019]). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to modify Horst's method as taught by Klein so it would change the size of the seed value based on the error rate of the device. In doing so, i.e. by increasing the size of the seed value as the number of errors increases, the error rate can be lowered. Therefore, the data integrity improves.

As per claims 10 and 20, see arguments with respect to the rejection of claim 5. Claims 10 and 20 are also rejected based on the same rationale as the rejection of claim 5.

9. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horst in view of Slaight (USPN: 2005/0138171).

As per claim 11, Horst teaches a system having a circuitry capable of responding to a data read request for requested data as described above in the rejection of claim 1. However, Horst does not teach that the system further comprising a PCI-E bus and a buffer. Slaight, on the other hand, teaches a PCI-E (Peripheral Component Interconnect-Express) bus (i.e. 212 in Figs. 2-3); and a buffer (i.e. 216 in Figs. 2-3) communicatively coupled to the PCI-E bus for temporarily storing the data received via PCI-E, the buffer being divided into at least one memory chunk (e.g. see Figs. 2-3). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of

the current invention was made to include the PCI-E bus and a buffer as taught by Slaight in the system taught by Horst so the data can be transferred at high speed between different components of the system via the PCI-E bus and the data can be temporarily stored in the buffer as taught by Slaight.

As per claim 12, the combination of Horst and Slaight teaches the claimed invention as described above and furthermore, Horst teaches that the validating the integrity of a given one of the at least one write transaction comprises, for a given memory chunk: determining if the memory chunk includes the seed value (i.e. the CRC bits); and if the memory chunk includes the seed value, determining that a transmission error occurred (i.e. by checking the CRC bits and declaring the transmission error if the CRC bits do not match) (e.g. see Col. 5, lines 44-47).

As per claim 13, the combination of Horst and Slaight teaches the claimed invention as described above and furthermore, Horst teaches that the determining if the memory chunk includes the seed value comprises determining if the memory chunk (i.e. the area of the memory) includes the seed value (i.e. the CRC bits) at specified bits (i.e. the 4-bytes at the LSB side, "CRC" field as shown in Fig. 3A) of the memory chunk (e.g. see Fig. 3A and Col. 17, lines 19-23).

As per claim 14, the combination of Horst and Slaight teaches the claimed invention as described above and furthermore, Horst teaches that the method additionally comprising modifying the seed value (i.e. recalculating the CRC bits) if it is determined that a transmission error occurred (e.g. see Col. 22, line 65 – Col. 23, line 11).

10. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horst in view of Slaight, further in view of Klein.

As per claim 5, the combination of Horst and Slaight teaches the claimed invention as described above. However, both Horst and Slaight failed to teach that the size of the seed value is based on a specified error rate of the device. Klein, on the other hand, teaches that the size of the seed value (i.e. the number of check bits) is based on a specified error rate of the device (i.e. the number of errors) (e.g. see paragraph [0019]). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to modify the method of Horst and Slaight as taught by Klein so it would change the size of the seed value based on the error rate of the device. In doing so, i.e. by increasing the size of the seed value as the number of errors increases, the error rate can be lowered. Therefore, the data integrity improves.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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